# Series Triacs In AC High Voltage Switching Circuits

**By George Templeton**
**Thyristor Applications Engineer**

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

## INTRODUCTION

**Edited and Updated**

This paper describes the series connection of triacs to create a high voltage switch suitable for operation at voltages up to 2000 Volts. They can replace electromechanical contactors or extend their current rating and lifetime. Motor starters and controllers operating at line voltages of 240 Volts or more require high-voltage switches. Transformer action and resonant snubber charging result in voltages much greater than the peak of the line. Triacs can be subjected to both commutating and static dV/dt when multiple switching devices are present in the circuit. Snubber designs to prevent static dV/dt turn-on result in higher voltages at turn-off. Variable load impedances also raise voltage requirements.

The benefits of series operation include: higher blocking voltage, reduced leakage, better thermal stability, higher dV/dt capability, reduced snubber costs, possible snubberless operation, and greater latitude in snubber design. The advantages of triacs as replacements for relays include:

- Small size and light weight
- Safety — freedom from arcing and spark initiated explosions
- Long lifespan — contact bounce and burning eliminated
- Fast operation — turn-on in microseconds and turn-off in milliseconds
- Quiet operation

Triacs can be used to replace the centrifugal switch in capacitor start motors. The blocking voltage required of the triac can be much greater than the line voltage would suggest. It must block the vector sum of the line, auxiliary winding, and start capacitor voltage. This voltage increases when triac turn-off occurs at higher rpm.

## TRIGGERING

Figure 1 illustrates a series thyristor switching circuit. In this circuit, the top triac triggers in Quadrant 1 when the bottom triac triggers in Quadrant 3. When the optocoupler turns on, gate current flows until the triacs latch. At that time, the voltage between the gate terminals drops to about 0.6 Volts stopping the gate current. This process repeats each half cycle. The power rating of the gate resistor can be small because of the short duration of the gate current. Optocoupler surge or triac gate ratings determine the minimum resistance value. For example, when the maximum optocoupler $I_{TSM}$ rating is 1 A:

$$R_g >= V_{peak}/I_{max} \quad (1.0)$$

$$R_g = 750\ V/1\ A = 750\ Ohm$$

The triacs retrigger every half cycle as soon as the line voltage rises to the value necessary to force the trigger current. The instantaneous line voltage V is

$$V = I_{GT}\ R_g + 2\ V_{GT} + 2\ V_{TM} \quad (1.1)$$

where $V_{GT}$, $I_{GT}$ are data book specifications for the triac and $V_{TM}$ is the on-voltage specification for the optocoupler.

The phase delay angle is

$$\theta_d = SIN^{-1}\left[\frac{V}{\sqrt{2}\ V_{LINE}}\right] \quad (1.2)$$

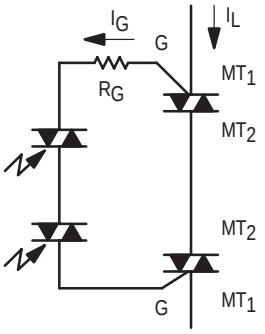



**Figure 6.1. Series Switch**

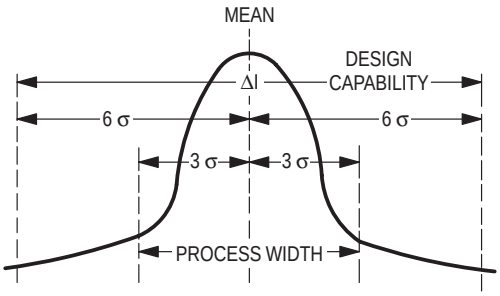



**Figure 6.2. Designing for Probable Leakage**

## STATIC VOLTAGE SHARING

Maximum blocking voltage capability results when the triacs share voltage equally. The blocking voltage can be dc or ac. A combination of both results when the triac switches the start winding in capacitor start motors. In the simple series connection, both triacs operate with an identical leakage current which is less than that of either part operated alone at the same voltage. The voltages across the devices are the same only when their leakage resistances are identical. Dividing the voltage by the leakage current gives the leakage resistance. It can range from 200 kohm to 2000 megohm depending on device characteristics, temperature, and applied voltage.

Drawing a line corresponding to the measured series leakage on each device's characteristic curve locates its operating point. Figure 3a shows the highest and lowest leakage units from a sample of 100 units. At room temperature, a leakage of 350 nA results at 920 Volts. The lowest leakage unit blocks at the maximum specified value of 600 Volts, while the highest blocks 320 Volts. A 50 percent boost results.

Figure 3b shows the same two triacs at rated $T_J max$. The magnitude of their leakage increased by a factor of about 1000. Matching between the devices improved, allowing operation to 1100 Volts without exceeding the 600 Volt rating of either device.

Identical case temperatures are necessary to achieve good matching. Mounting the devices closely together on a common heatsink helps.

A stable blocking condition for operation of a single triac with no other components on the heatsink results when

$$\frac{dI_{MT}}{dT_J} \cdot \frac{dT_J}{dP_J} \cdot \frac{dP_J}{dI_{MT}} < 1 \qquad (2.0)$$

Thermal run-away is a regenerative process which occurs whenever the loop gain in the thermal feedback circuit reaches unity. An increase in junction temperature causes increased leakage current and higher power dissipation. Higher power causes higher junction temperature which in turn leads to greater leakage. If the rate of heat release at the junction exceeds the rate of removal as temperature increases, this process repeats until the leakage current is sufficient to trigger the thyristor on.

DC blocking simplifies analysis. A design providing stable dc operation guarantees ac performance. AC operation allows smaller heatsinks.

The last term in the stability equation is the applied voltage when the load resistance is low and the leakage causes negligible voltage drop across it. The second term is the thermal resistance from junction to ambient. The first term describes the behavior of leakage at the operating conditions. For example, if leakage doubles every 10°C, a triac operating with 2 mA of leakage at 800 Vdc with a 6°C/W thermal resistance is stable because

$$\frac{2\ mA}{10°C} \cdot \frac{6°C}{W} \cdot 800\ V = 0.96$$

Operating two triacs in series improves thermal stability. When two devices have matched leakages, each device sees half the voltage and current or 1/4 of the power in a single triac. The total leakage dissipation will approach half that of a single device operated at the same voltage. The additional voltage margin resulting from the higher total blocking voltage reduces the chance that either device will operate near its breakdown voltage where the leakage current increases rapidly with small increments in voltage. Higher voltage devices have lower leakage currents when operated near breakdown. Consequently, the highest breakover voltage unit in the pair will carry the greatest proportion of the burden. If the leakage current is large enough to cause significant changes in junction temperature, ($\Delta T_J = \phi_{JC} P_D$), the effect will tend to balance the voltage division between the two by lowering the leakage resistance of the hotter unit. If the leakage mismatch between the two is large, nearly all the voltage will drop across one device. As a result there will be little benefit connecting two in series.

Series blocking voltage depends on leakage matching. Blocking stability depends on predictable changes in leakage with temperature. Leakage has three components.

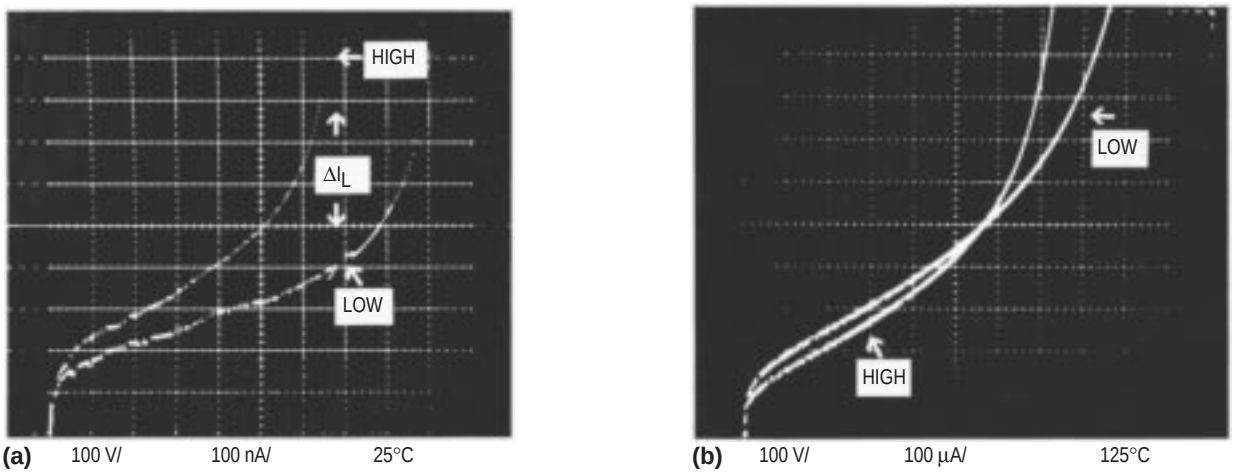



**Figure 6.3. Leakage Matching versus Temperature**

### Surface Leakage

Passivation technique, junction design, and cleanliness determine the size of this component. It tends to be small and not very dependent on temperature.

### Diffusion Leakage

Measurements with 1 volt reverse bias show that this component is less than 10 percent of the total leakage for allowed junction temperatures. It follows an equation of the form:

$$I \propto e^{-(qv/kT)} \qquad (2.1)$$

and doubles about every 10°C. Its value can be estimated by extrapolating backward from high temperature data points.

### Depletion Layer Charge Generation

This component is a result of carriers liberated from within the blocking junction depletion layer. It grows with the square root of the applied voltage. The slope of the leakage versus applied voltage is the mechanism allowing for series operation with less than perfect leakage matching. Predictable diffusion processes determine this leakage. At temperatures between 70 and 150°C it is given by:

$$i \propto e^{-\frac{E}{kT}} \qquad (2.2)$$

where E = 1.1 eV, k = 8.62E – 5 eV/k, T = degrees Kelvin, and k = 8.62 x $10^{-5}$ eV/k.

It is useful to calculate the percentage change in leakage current with temperature:

$$A = \frac{1}{i}\frac{di}{dT_J} = \frac{E}{kT^2} = 0.08 = \frac{8\%}{°C}$$

The coefficient A was evaluated on 3 different die size triacs by curve fitting to leakage measurements every 10° from 70 to 150°C. Actual values measured 0.064 at 125° and 0.057 at 150°.

Deviations from this behavior will result at voltages and temperatures where leakage magnitude, current gain, and avalanche multiplication aid unwanted turn-on. Sensitive gate triacs are not recommended for this reason.

## DERATING AND LEAKAGE MATCHING

Operation near breakdown increases leakage mismatch because of the effects of avalanche multiplication. For series operation, devices should be operated at least 100 Volts below their rating.

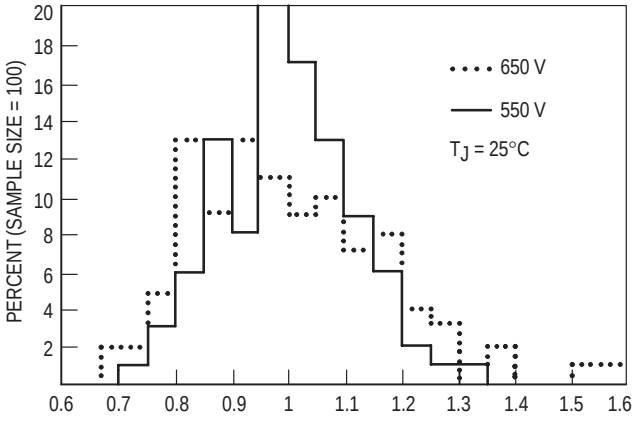



**Figure 6.4. Normalized Leakage (Mean = 1.0)**

Figure 4 shows the leakage histogram for a triac sample operated at two different voltages. The skewedness in the high-voltage distribution is a consequence of some of the sample operating near breakdown.

## HEATSINK SELECTION

Solving equations (2.0) and (2.3) for the thermal resistance required to prevent runaway gives:

$$\theta_{JA} < \frac{1}{A \cdot V \cdot i} \quad (3.0)$$

where $\theta_{JA}$ is thermal resistance, junction to ambient, in °C/W, A = 0.08 at $T_J$ = 125°C, V = rated $V_{DRM}$, and i = rated $I_{DRM}$.

$\theta_{JA}$ must be low enough to remove the heat resulting from conduction losses and insure blocking stability. The latter can be the limiting factor when circuit voltages are high. For example, consider a triac operated at 8 amps (rms) and 8 Watts. The allowed case temperature rise at 25° ambient is 85°C giving a required $\theta_{CA}$ (thermal resistance, case to ambient) of 10.6°C/W. Allowing 1°C/W for $\theta_{CHS}$ (thermal resistance, case to heatsink) leaves 9.6°C/W for $\theta_{SA}$ (thermal resistance, heatsink to ambient). However, thermal stability at 600 V and 2 mA $I_{DRM}$ requires $\theta_{JA}$ = 10.4°C/W. A heatsink with $\theta_{SA}$ less than 7.4°C/W is needed, given a junction to case thermal resistance of 2°C/W.

The operation of devices in series does not change the coefficient A. When matching and thermal tracking is perfect, both devices block half the voltage. The leakage current and power divide by half and the allowed $\theta_{JA}$ for blocking stability increases by 4.

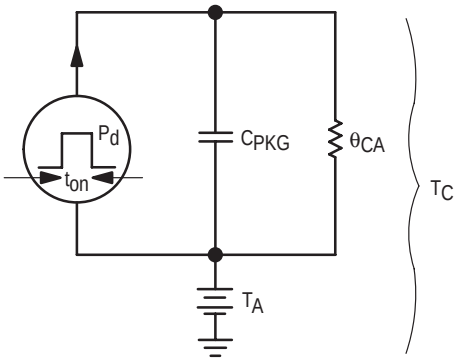
Low duty cycles allow the reduction of the heatsink size. The thermal capacitance of the heatsink keeps the junction temperature within specification. The package time constant ($C_{pkg} R_{\theta JA}$) is long in comparison with the thermal response time of the die, causing the instantaneous $T_J$ to rise above the case as it would were the semiconductor mounted on an infinite heatsink. Heatsink design requires estimation of the peak case temperature and the use of the thermal derating curves on the data sheet. The simplest model applies to a very small heatsink which could be the semicondutor package itself. When $\theta_{SA}$ is large in comparison with $\theta_{CHS}$, it is sufficient to lump both the package and heatsink capacitances together and treat them as a single quantity. The models provide good results when the heatsink is small and the thermal paths are short.

Model C, Figure 5 is a useful simplification for low duty cycle applications. Increasing heatsink mass adds thermal capacitance and reduces peak junction temperature. Heatsink thermal resistance is proportional to surface area and determines the average temperature.

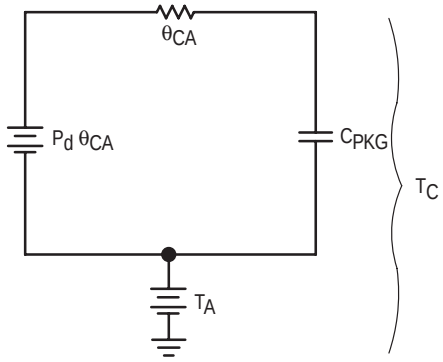
$$\theta_{SA} = 32.6\ A^{(-0.47)} \quad (3.1)$$

where A = total surface area in square inches, $\theta_{SA}$ = thermal resistance sink to ambient in °C/W.

Analysis of heatsink thermal response to a train of periodic pulses can be treated using the methods in ON Semiconductor application note AN569 and Figure 6. For example:




**(a.) Standard Thermal Analogue For a Thyristor in Free Air**




**(b.) Equivalent Circuit For (a)**

In Circuit (B):

The steady state case temperature is given by

(5.0) $$T_{CSS} = P_d\ \theta_{CA} + T_A \text{ in } °C$$

where $P_d$ = Applied average power, watts
$\theta_{CA}$ = Case to ambient thermal resistance, °C/W
$T_A$ = ambient temperature, °C

The package rises toward the steady state temperature exponentially with time constant

(5.1) $$\tau = \theta_{CA}\ C_{PKG},\ \text{seconds}$$

where $C_{pkg}$ = HM, Joules/°C
H = Specific heat, calories/(gm • °C)
M = Mass in grams
and 1 Calorie = 4.184 Joule
1 Joule = 1 Watt • Sec

The case temperature rise above ambient at the end of power pulse is:

(5.2) $$\Delta T_{C_{pk}} = \Delta T_{CSS}(1 - e^{-t_{on}/\tau})$$

where $\Delta T_{C_{pk}} = T_{C_{pk}} - T_A$

$\Delta T_{CSS} = T_{CSS} - T_A$

To account for thermal capacity, a time dependent factor r(t) is applied to the steady state case-to-ambient thermal resistance. The package thermal resistance, at a given on-time, is called transient thermal resistance and is given by:

$$R_{\theta CA}\ (t_{on}) = r(t_{on})\ \theta_{CA}$$

where $r(t_{on})$ = Unitless transient thermal impedance coefficient.

In terms of measurable temperatures:

(5.3) $$r(t_{on}) = \frac{\Delta T_{C_{pk}}}{\Delta T_{CSS}}$$

In model (b.) this is

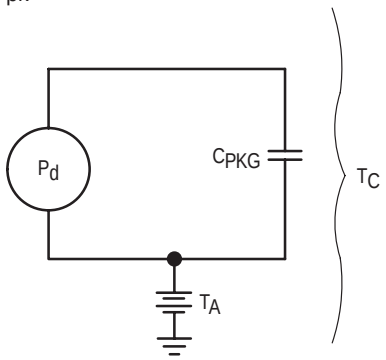
(5.4) $$r(t_{on}) = (1 - e^{-t_{on}/\tau})$$

Solving 5-4 for the package capacitance gives

(5.5) $$C_{PKG} = \frac{-t_{on}}{(\theta_{CA}\ \ln\ (1 - r(t_{on}))}$$

Use simplified model C when

$t_{on} << \tau$
$\Delta T_{C_{pk}} << \Delta T_{CSS}$




**(c.) Simplified Model**

(5.6) $$T_C = \frac{P_d\ t_{on}}{C_{PKG}} + T_A$$

**Figure 6.5. Transient Thermal Response For a Single Power Pulse**

Assume the case temperature changes by 40°C for a single power pulse of 66.67 W and 3 s duration. Then from equation (5.6):

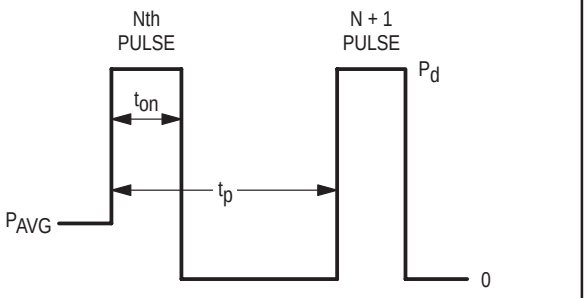
$$C_{pkg} = \frac{(66.7\ \text{Watts})\ (3\ \text{seconds})}{40°C} = \frac{5\ \text{Joules}}{°C}$$

The heatsink thermal resistance can be determined by applying dc power, measuring the final case temperature, and using equation (5.0).

$$\frac{T_C - T_A}{P_D} = \frac{175\text{-}25}{5} = 30°C/W$$

The application requires a 3 s on-time and 180 s period at 66.7 W. Then

$$P_{avg} = (66.7\ W)\ (3/180) = 1.111\ W$$




$$\Delta T_C\ (N + 1) = [P_{AVG} + (P_d - P_{AVG})\ r(t_{on} + t_p) + P_d\ r(t_{on}) - P_d\ r(t_p)]\theta_{CA}$$

Where $\Delta T_C$ (N + 1) = maximum rise above ambient
$P_d$ = applied average power within a pulse
$P_{AV\ G}$ = average power within a period
$r(t_{on} + t_p)$ = time dependent factor for sum of $t_{on}$ and $t_p$
$r(t_{on})$ = time dependent factor for $t_{on}$
$r(t_p)$ = time dependent factor for $t_p$

**Figure 6.6. Steady State Peak Case Temperature Rise**

Using equation (5.3), the theoretical steady state case temperature rise is:

$$T_{CSS} - T_A = (66.7\ W)\ (30°C/W) = 2000°C$$

and

$$R(t_{on}) = R\ (3\ s) = (40°C\ \text{measured rise})/2000 = 0.02$$

From equation (5.4) and (5.1):

$$R\ (T_p) = (1 - e^{-180/150}) = .6988$$

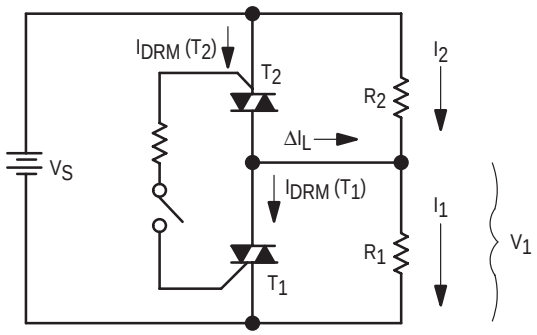
$$R\ (t_{on} + Tp) = (1 - 1^{-183/150}) = .7047$$

Then from Figure 6:
delta $T_C$ = (1.111 + 46.225 + 1.333 – 46.61) 30 = 61.8°C
If the ambient temperature is 25°C, $T_C$ = 87°C.

## COMPENSATING FOR MAXIMUM SPECIFIED LEAKAGE

Identical value parallel resistors around each triac will prevent breakdown resulting from mismatched leakages. Figure 7 derives the method for selecting the maximum allowed resistor size. A worst case design assumes that the series pair will operate at maximum $T_J$ and that one of the triacs leaks at the full specified value while the other has no leakage at all. A conservative design results when the tolerances in the shunt resistors place the highest possible resistor across the low leakage unit and the lowest possible resistor around the high leakage unit.

This method does not necessarily provide equal voltage balancing. It prevents triac breakover. Perfect voltage sharing requires expensive high-wattage resistors to provide large bleeder currents.




$$V_1 = \frac{V_S R_1}{R_1 + R_2} + \frac{\Delta I_L R_1 R_2}{R_1 + R_2}$$

Let $R_1 = R\ (1 + p)$ and $R_2 = R\ (1 - p)$ where
R = Nominal resistor value
p = 0.05 for 5% tolerance, etc.

$$R \leqq \frac{2\ V_{DRM} - V_S\ (1 + p)}{\Delta I_L\ (1 - p^2)}$$

Worst case becomes:

and $I_{DRM}\ (T_1) = 0$; $I_{DRM}\ (T_2)$ = Spec. max. value
$\Delta I_L$ = Spec. Max. Value

**Figure 6.7. Maximum Allowed Resistor for Static Voltage Sharing**

## COMPENSATION FOR PROBABLE LEAKAGE

Real triacs have a leakage current greater than zero and less than the specified value. Knowledge of the leakage distribution can be used to reduce resistor power requirements. The first step is to statistically characterize the product at maximum temperature. Careful control of the temperature is critical because leakage depends strongly on it.

The process width is the leakage span at plus or minus 3 standard deviations (sigma) from the mean. To minimize the probability of out of spec parts, use a design capability index (Cp) of 2.0.

$$C_p = (\text{design } \Delta I)/(\text{process width}) \qquad (4.0)$$

$$Cp = (12 \text{ sigma})/(6 \text{ sigma})$$

Figure 2 and Figure 7 describe this. Substituting delta $I_L$ at 6 sigma in Figure 7 gives the resistor value. The required power drops by about 4.

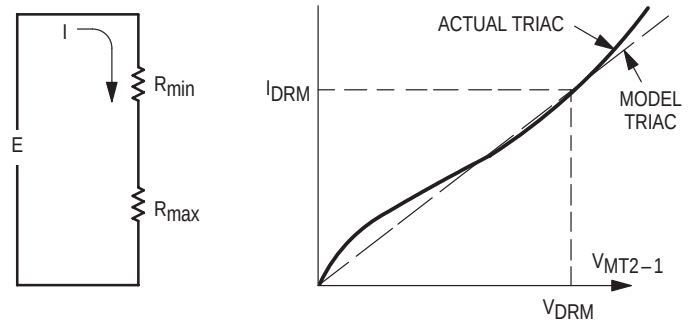
Theoretically there would be no more than 3.4 triacs per million exceeding the design tolerance even if the mean value of the leakage shifted by plus or minus 1.5 sigma.

## SELECTING RESISTORS

Small resistors have low voltage ratings which can impose a lower constraint on maximum voltage than the triac. A common voltage rating for carbon resistors is:

| Rated Power (W) | Maximum Voltage (V) |
|---|---|
| 1/4 Watt | 250 Volts |
| 1/2 | 350 |
| 1 | 500 |
| 2 | 750 |

Series resistors are used for higher voltage.




(a) Equivalent Circuit (b) Model

$$\text{Let } V_{DRM} = E\,\frac{R_{max}}{R_{max} + R_{min}}$$

$$E = V_{DRM}\left(1 + \frac{I_{min}}{I_{max}}\right)$$

$$R_{max} = \frac{V_{DRM}}{I_{min}} \qquad R_{min} = \frac{V_{DRM}}{I_{max}} \qquad (8.0)$$

**Figure 6.8. Maximum Voltage Sharing Without Shunt Resistor**

## OPERATION WITHOUT RESISTORS

Figure 8 derives the method for calculating maximum operating voltage. The voltage boost depends on the values of $I_{min}$ and $I_{max}$. For example :

$$\left(1 + \frac{131\ \mu A}{683\ \mu A}\right) = 1.19$$

A 19 percent voltage boost is possible with the 6 sigma design. Testing to the measured maximum and minimum of the sample allows the boost to approach the values given in Table 1.

$$(1 + 0.835/1.228) = 1.68$$

**Table 1. Normalized leakage and voltage boost factor. (Mean = 1.0)**

| Voltage (V) | 550 | 650 | 550 | 550 | 550 | 550 | 550 |
|---|---|---|---|---|---|---|---|
| $T_J$ (°C) | 25 | 25 | 100 | 125 | 125 | 150 | 150 |
| $R_{shunt}$ | — | — | — | — | 1.5M | 1.5M | 510K |
| Sample Size | 100 | 100 | 16 | 16 | 16 | 16 | 16 |
| Maximum | 1.315 | 1.591 | 1.187 | 1.228 | 1.123 | 1.346 | 1.186 |
| Minimum | 0.729 | 0.681 | 0.840 | 0.835 | 0.920 | 0.820 | 0.877 |
| Sigma | 0.116 | 0.172 | 0.106 | 0.113 | 0.055 | 0.132 | 0.084 |
| Sample Boost | 1.55 | 1.43 | 1.71 | 1.68 | 1.82 | 1.61 | 1.74 |
| 6 Sigma Boost | 1.18 | 1.00 | 1.22 | 1.19 | 1.50 | 1.12 | 1.33 |

## COMPENSATING FOR SURFACE LEAKAGE

A small low power shunt resistance will provide nearly perfect low temperature voltage sharing and will improve high temperature performance. It defines the minimum leakage current of the parallel triac-resistor combination. The design method in Figure 8 can be used by adding the resistor current to the measured maximum and minimum leakage currents of the triac sample. This is described in Table 1.

## SERIES $\left(\frac{dV}{dt}\right)_s$

The series connection will provide twice the $\left(\frac{dV}{dt}\right)_s$ capability of the lowest device in the pair (Figure 9).

Dynamic matching without a snubber network depends on equality of the thyristor self capacitance. There is little variation in junction capacitance. Device gain variations introduce most of the spread in triac performance.

The blocking junction capacitance of a thyristor is a declining function of dc bias voltage. Mismatch in static blocking voltage will contribute to unequal capacitances. However, this effect is small at voltages beyond a few volts. The attachment of a heatsink at the high-impedance node formed by connection of the triac main-terminals can also contribute to imbalance by introducing stray capacitance to ground. This can be made insignificant by adding small capacitors in parallel with the triacs. Snubbers will serve the same purpose.

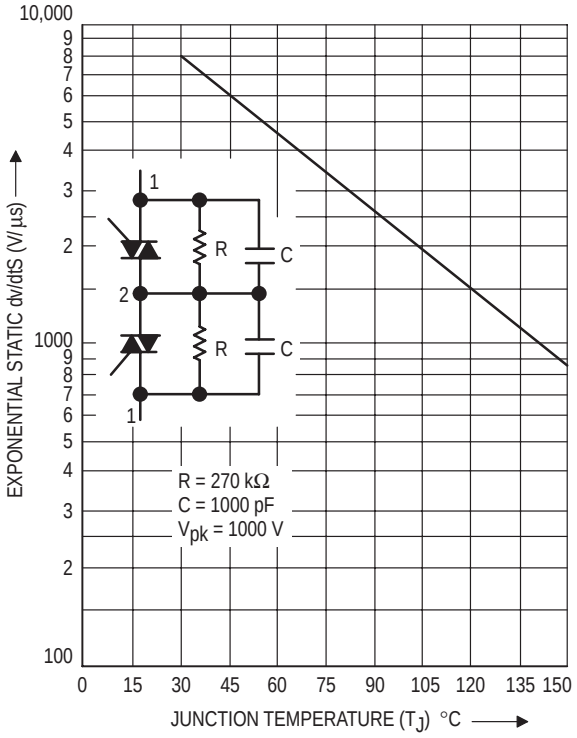



**Figure 6.9. Exponential Static dV/dt, Series MAC15-8 Triacs**

Triacs can tolerate very high rates of voltage rise when the peak voltage magnitude is below the threshold needed to trigger the device on. This behavior is a consequence of the voltage divider action between the device collector and gate-cathode junction capacitances. If the rise-time is made short in comparison with minority carrier lifetime, voltage and displaced charge determine whether the device triggers on or not. Series operation will extend the range of voltage and load conditions where a static $\frac{dV}{dt}$ snubber is not needed.

Figure 10 graphs the results of measurements on two series connected triacs operated without snubbers. The series connection doubled the allowed step voltage. However, this voltage remained far below the combined 1200 V breakover voltage of the pair.

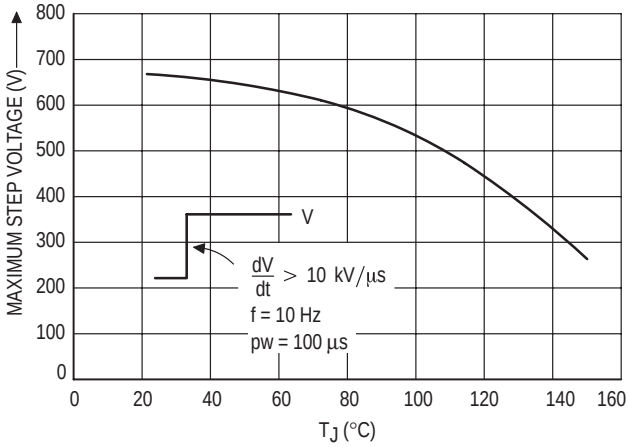



**Figure 6.10. Step Blocking Voltage $V_S$ $T_J$ (Unsnubbed Series Triacs)**

Exponential $\left(\frac{dV}{dt}\right)_s$ tests performed at 1000 V and less than 2 kV/μs showed that turn-on of the series pair can occur because of breakdown or $\frac{dV}{dt}$. The former was the limiting factor at junction temperatures below 100°C. Performance improved with temperature because device gain aided voltage sharing. The triac with the highest current gain in the pair is most likely to turn-on. However, this device has the largest effective capacitance. Consequently it is exposed to less voltage and $\frac{dV}{dt}$. At higher temperatures, rate effects dominated over voltage magnitudes, and the capability of the series pair fell. $\frac{dV}{dt}$ performance of the series devices was always better than that of a single triac alone.

## TURNOFF

Process tolerances cause small variations in triac turn-off time. Series operation will allow most of the reapplied blocking voltage to appear across the faster triac when a dynamic voltage sharing network is not used.

Figure 11 describes the circuit used to investigate this behavior. It is a capacitor discharge circuit with the load series resonant at 60 Hz. This method of testing is desirable because of the reduced burn and shock hazard resulting from the limited energy storage in the load capacitor.

The triacs were mounted on a temperature controlled hotplate. The single pulse non-repetitive test aids junction temperature control and allows the use of lower power rated components in the snubber and load circuit.

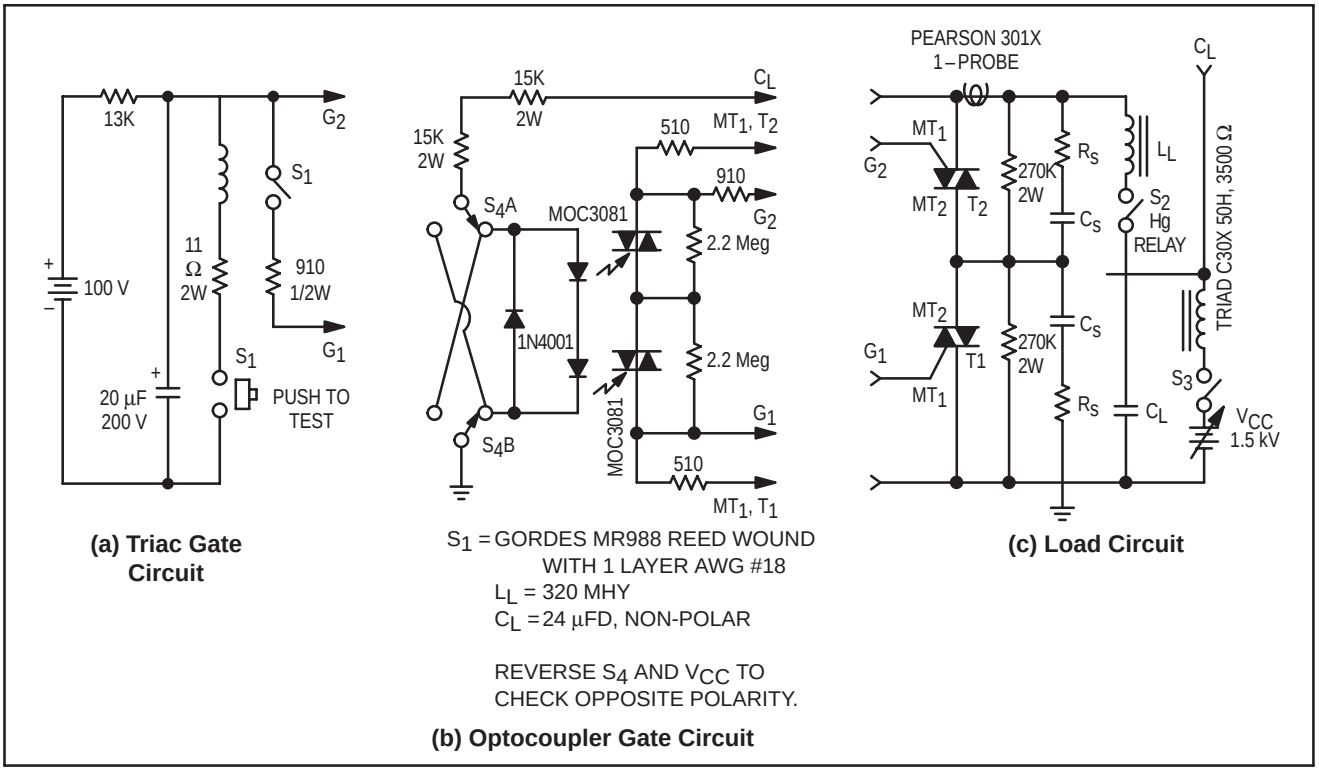



**Figure 6.11.** $\left(\frac{dV}{dt}\right)_c$ **Test Circuit**

Snubberless turn-off at 1200 V and 320 milli-henry resulted in 800 V peak and 100 V/µs. Although this test exceeded the ratings of the triacs, they turned off successfully.

Snubberless operation is allowable when:

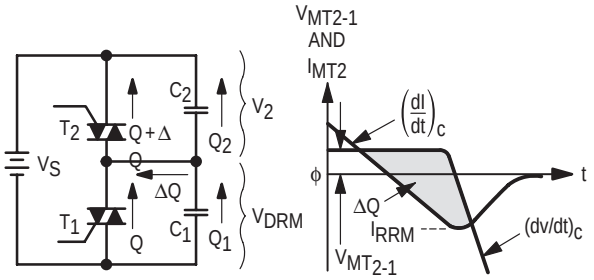
1. The total transient voltage across both triacs does not exceed the rating for a single device. This voltage depends on the load phase angle, self capacitance of the load and triac, damping constant, and natural resonance of the circuit.
2. The total $\left(\frac{dV}{dt}\right)_c$ across the series combination does not exceed the capability of a single device.

Maximum turn-off voltage capability and tolerance for variable loads requires the use of a snubber network to provide equal dynamic voltage sharing. Figure 12 and Figure 13 derives the minimum size snubber capacitor allowed. It is determined by the recovery charge of the triac. Measurements in fast current crossing applications suggest that the reverse recovery charge is less than 2 micro-coulombs. Recovery currents cannot be much greater than $I_H$ or $I_{GT}$, or the triac would never turn-off. Recovery can be forward, reverse, or near zero current depending on conditions.

Snubber design for the series switch has the following objectives:

- Controlling the voltage peak. Resonant charging will magnify the turn-off voltage.
- Controlling the voltage rate. Peak voltage trades with voltage rate.
- Equalizing the voltage across the series devices by providing for imbalance in turn-off charge.

Designs that satisfy the first two objectives will usually provide capacitor values above the minimum size. Select the snubber for a satisfactory compromise between voltage and $\frac{dV}{dt}$. Then check the capacitor to insure that it is sufficiently large.




Worst case:

$C_2 = C(1 + p)$; $C_1 = C(1 - p)$; $Q_1 = 0$; $Q_2 = \Delta Q$

where C = Nominal value of capacitor
and p = 0.1 for 10% tolerance, etc.
ΔQ = Reverse recovery charge

Note that $T_1$ has no charge while $T_2$ carries full recovery charge.

For the model shown above,

$$V_S = \frac{Q_1}{C_1} + \frac{Q_2}{C_2} = \frac{Q_1}{C(1 - p)} + \frac{Q_1 - \Delta Q}{C(1 + p)}$$

$$C \geqq \frac{\Delta Q}{2\ V_{DRM} - V_S(1 + p)}$$

**Figure 6.12. Minimum Capacitor Size for Dynamic Voltage Sharing**

Snubber designs for static, commutating, and combined $\frac{dV}{dt}$ stress are shown in Table 2. Circuits switching the line or a charged capacitor across a blocking triac require the addition of a series snubber inductor. The snubber must be designed for maximum $\frac{dV}{dt}$ with the minimum circuit inductance. This contraint increases the required triac blocking voltage.

**Table 2. Snubber Designs**

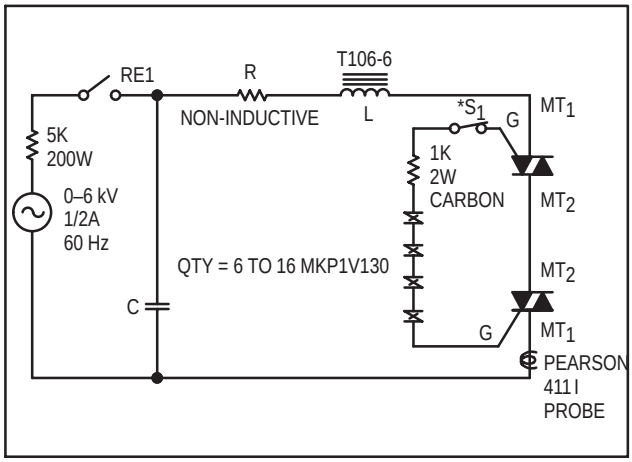
| Type | $\left(\frac{dV}{dt}\right)_c$ | $\left(\frac{dV}{dt}\right)_s$ | Both |
|---|---|---|---|
| L (mh) | 320 | 0.4 | 320 |
| $R_L$ Ohm | 8 | 0 | 8 |
| $R_S$ Ohm | 1820 | 48 | 48 |
| $C_S$ (μf) | 0.5 | 0.5 | 0.5 |
| Damping Ratio | 1.14 | 0.85 | .035 |
| $V_{step}$ (V) | 1200 | 1200 | 750 |
| $V_{pk}$ (V) | 1332 | 1400 | 1423 |
| $t_{pk}$ (μs) | 768 | 29.8 | 1230 |
| $\frac{dV}{dt}$ (V/μs) | 4.6 | 103 | 1.3 |

Note: Divide $R_S$ and $\frac{dV}{dt}$ by 2, multiply $C_S$ by 2 for each triac.

## $\frac{dI}{dt}$ CAPABILITY

The hazard of thyristor damage by $\frac{dI}{dt}$ overstress is greater when circuit operating voltages are high because $\frac{dI}{dt}$ is proportional to voltage. Damage by short duration transients is possible even though the pulse is undetectable when observed with non-storage oscilloscopes. This type of damage can be consequence of snubber design, transients, or parasitic capacitances.

A thyristor can be triggered on by gate current, exceeding its breakdown voltage, or by exceeding its $\left(\frac{dV}{dt}\right)_s$ capability. In the latter case, a trigger current is generated by charging of the internal depletion layer capacitance in the device. This effect aids turn-on current spreading, although damage can still occur if the rate of follow on $\frac{dI}{dt}$ is high. Repetitive operation off the ac line at voltages above breakdown is a worst case condition. Quadrant 3 has a slightly slower gated turn-on time, increasing the chance of damage in this direction. Higher operating voltages raise power density and local heating, increasing the possibility of die damage due to hot-spots and thermal run-away.




| Vci V | C μFD | L μHY | R Ω | dI/dt A/μs | Rejects Tested |
|---|---|---|---|---|---|
| 1000 | 4.06 | 3.4 | 5.7 | 100 | 0/100 |
| 1900* | 1.05 | 7.9 | 5.7 | 179 | 0/195 |
| 1500 | 0.002 | 0.3 | 10 | 3000 | 3/10 |

* Open $S_1$ to test breakover dI/dt

**Figure 6.13. dI/dt Test Circuit**

Ideally, turn-on speed mismatch should not be allowed to force the slower thyristor into breakdown. An RC snubber across each thyristor prevents this. In the worst case, one device turns on instantly while the other switches at the slowest possible turn-on time. The rate of voltage rise at the slower device is roughly $\frac{dV}{dt} = \frac{V_I R_S}{2L}$, where $V_I$ is the maximum voltage across L. This rate should not allow the voltage to exceed $V_{DRM}$ in less than $T_{gt}$ to prevent breakover. But what if the thyristors are operated without a snubber, or if avalanche occurs because of a transient overvoltage condition?

The circuit in Figure 13 was constructed to investigate this behavior. The capacitor, resistor, and inductor create a pulse forming network to shape the current wave. The initial voltage on the capacitor was set by a series string of sidac bidirectional breakover devices.

Test results showed that operation of the triac switch was safe as long as the rate of current rise was below 200 A/μs. This was true even when the devices turned on because of breakover. However, a 0.002 μf capacitor with no series limiting impedance was sufficient to cause damage in the Q3 firing polarity.

Circuit malfunctions because of breakover will be temporary if the triac is not damaged. Test results suggest that there will be no damage when the series inductance is sufficient to hold dl/dt to acceptable values. Highly energetic transients such as those resulting from lightning strikes can cause damage to the thyristor by $I^2t$ surge overstress. Device survival requires the use of voltage limiting devices in the circuit and $\frac{dV}{dt}$ limiting snubbers to prevent unwanted turn-on. Alternatively, a large triac capable of surviving the surge can be used.

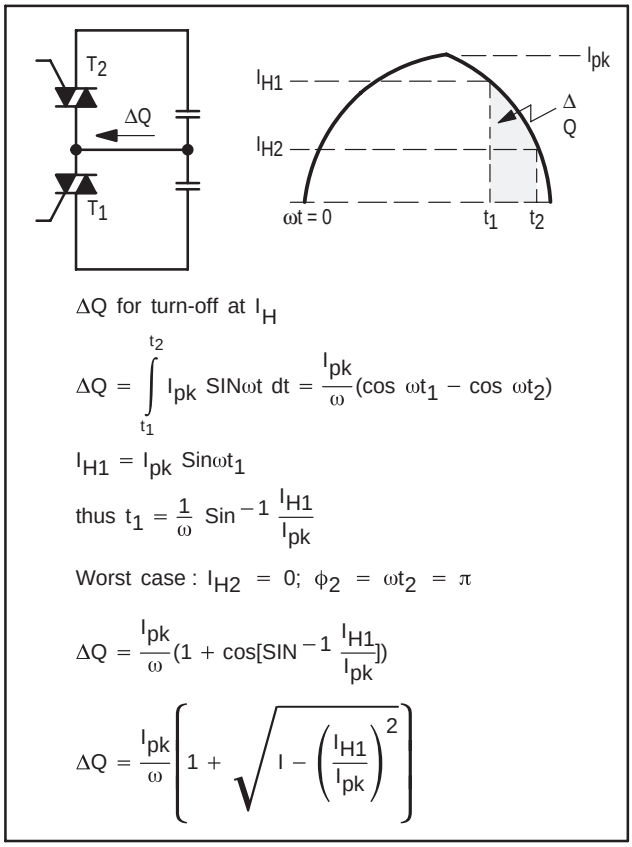



**Figure 6.14. Forward Recovery Charge for Turn-Off at $I_H$**

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